HW 4 - Binary Multiplier

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**Theory**

Binary multiplication is multiplication of two binary numbers. We can simplify this to the sum of multiplying each bit in the second input by the first input, accounting for a possible left-shift which multiplies by 2. Because each bit of the second input is either a 0 or a 1, we can simply use an AND gate between each bit of the first input and the bit in question from the second input to determine the value of the term that we are finding in this step. Once we use the AND gate for this term, we add this to the term generated by multiplying by the second least significant bit, with a left-shift of 1 bit (multiplying by 210 in binary), and successively doing this until we reach the most significant bit of the second term, while still including the left-shifts for each term we are summing. This way we can reduce a multiplication to using AND gates and adders.

**Test Cases**

| A | B | A\*B |
| --- | --- | --- |
| 000 | 0000 | 0000000 |
| 000 | 1111 | 0000000 |
| 111 | 0000 | 0000000 |
| 101 | 0110 | 0011110 |
| 111 | 1111 | 1101001 |

| C0 | A1 | B1 | D | E | P1 | S1 | C0’D | C1 |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |

**Question**

There are 3 levels of gates within each addition part of each adder, so with 2 adders being used fully, the adders account for 3\*4\*2=24 levels of gates. There are also the delays from the AND gates, each of which has a 1-gate delay. Now, there are 25 levels of gates for each computation, and with the inverter, that leaves 26 gates. This leaves a 260 ns propagation delay for this 3-bit \* 4-bit adder.